

**WHAT IS CLAIMED IS:**

1. A method of forming a ferroelectric memory device, comprising:  
forming at least one capacitor pattern over a substrate, each capacitor pattern having an adhesive assistant pattern, a lower electrode, a ferroelectric pattern, and an upper electrode;  
forming an oxygen barrier layer over the substrate;  
etching the oxygen barrier layer to expose a sidewall of the ferroelectric pattern but not a sidewall of the adhesive assistant pattern; and  
performing a thermal process for curing ferroelectricity.
2. The method as claimed in claim 1, wherein the forming at least one capacitor pattern step comprises:  
sequentially forming an adhesive assistant layer, a lower electrode layer, a ferroelectric layer, and an upper electrode layer over a substrate; and  
patterning the sequentially formed layers to create each capacitor pattern.
3. The method as claimed in claim 1, wherein the oxygen barrier layer is formed to have a substantially uniform thickness over the substrate.
4. The method as claimed in claim 1, wherein the etching step is performed by anisotropically etching.
5. The method as claimed in claim 1, wherein the thermal process for

curing ferroelectricity is performed in an oxygen ambient at a temperature of 450 ~ 800°C for 30 minutes or less.

6. The method as claimed in claim 1, after performing the thermal process for curing the ferroelectricity, further comprising:

forming a hydrogen barrier layer over the substrate to cover each capacitor pattern; and

forming an interlayer dielectric layer over the hydrogen barrier layer to fill up a space between the capacitor patterns.

7. The method as claimed in claim 6, wherein the hydrogen barrier layer is formed of aluminum oxide.

8. The method as claimed in claim 1, after the forming an oxygen barrier layer step, further comprising:

forming a material layer over the oxygen barrier layer such that portions of the material layer between the capacitor patterns is thicker than portions of the material layer over a top of the capacitor patterns.

9. The method as claimed in claim 8, wherein the forming the material layer step is performed by at least one of:

stacking and reflowing the material layer,

stacking the material layer and performing a planarization-etching process, and

performing a blanket CVD process.

10. The method as claimed in claim 1, wherein the forming the oxygen barrier layer step is performed by one of a chemical vapor deposition (CVD), an atomic layer deposition (ALD), and a sputtering technique.

11. The method as claimed in claim 2, wherein the ferroelectric layer is formed through a crystallization process in an oxygen ambient at a temperature above 700°C by using one of a sol-gel transfer, a sputtering, and a CVD technique.